Project proposal

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Problem

With the advancement of technology and scaling down the transistor sizes, leakage current became one of the main sources for power consumption. Some circuits is affected by this more than others, SRAM in particular is affected drastically since typically it has huge amount of cells and most of the time those cells are static and only burning energy through leakage current. Any method to reduce this leakage can affect the integrity and the power consumption performance of the SRAM in a significant way.

Approach

Our approach for this problem is to look through four known techniques to reduce leakage current and evaluate each technique based on three main metrics, leakage reduction, size and number of transistors needed and the delay that technique has on the memory for reading and writing. We will try to give those techniques with three main “awards”, best leakage reduction, best leakage reduction/Size and least delay technique. While those three awards are the main goals, we will explore the techniques using different parameters to get a wider analysis of those techniques for the mainly the three metrics we mentioned and some additional metrics that might be interesting to explore once we do the simulations.

Design

We will use four known leakage reduction techniques on memory cells, the four techniques are: Sleep transistors, Stack transistors, zigzag transistors and sleepy stack transistors. A concept circuit of each technique will be presented later in the proposal. We will design our own memory cells using the four techniques using cadence tools. The four techniques been presented for typical circuits before, but not for SRAM memory cells.

Novelty

While reduction techniques been evaluated for their leakage reduction ability for simple circuits, we will focus our work on SRAM cells and we will explore more metrics than other previous comparisons of those techniques. While we are not inventing new technique, having a comprehensive comparison could potentially help future designers choose the best solution for their design without having to do the comparison themselves thus contributing to the advancement in this area.

Expected outcomes

We should end up with multiple graphs depicting the three metrics we chose. Each graph will show the trend of each technique based on the metric. While we don't have simulations at this point since we started later than other groups, we are expecting the trend of the simulations to be similar to the ones shown later in this proposal. We should end up with multiple tables summarizing the strong and the weak points of each technique as well.

Design component: Designing SRAM memory cells with the four leakage reduction techniques

Research component: Comparison of the techniques using more metrics than typical papers do and compare them for SRAM cells rather for simple circuits.

Simulations: While we cannot limit our simulations to those, but they will be included, leakage vs. size, delay of read, write of each technique and using different parameters of each technique, leakage current of each technique under different parameters with, of course, the base case simulations.

Task Schedule

1. Ruchir Puri et al., "Pushing ASIC performance in a power envelope," in *Proceedings of the 40th annual Design Automation Conference* (Anaheim, CA, USA: ACM, 2003), 788-793.
2. Zongjian Chen et al., "A 2× load/store pipe for a low-power 1-GHz embedded processor," *Solid-State Circuits, IEEE Journal of* 38, no. 11 (2003): 1857-1865.
3. N.S. Kim et al., "Leakage current: Moore's law meets static power," *Computer* 36, no. 12 (2003): 68-75.
4. Y. Shimazaki, R. Zlatanovici, and B. Nikolic, "A shared-well dual-supply-voltage 64-bit ALU," *Solid-State Circuits, IEEE Journal of* 39, no. 3 (2004): 494-500.
5. Kyeong-Sik Min et al., "Leakage-suppressed clock-gating circuit with Zigzag Super Cut-off CMOS (ZSCCMOS) for leakage-dominant sub-70-nm and sub-1-

V-VDD LSIs," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* 14, no. 4 (2006): 430-435.
6. J. C. Park and V. J. Mooney III, "Sleepy Stack Leakage Reduction," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on* 14, no. 11 (2006): 1250-1263.
7. Leakage control with efficient use of transistor stacks in single threshold CMOS. M. Johnson, D. Somasekhar, L.-Y. Chiou, K. Roy. IEEE Transactions on VLSI Systems, February 2002.
8. A Leakage Reduction Methodology for Distributed MTCMOS. B. H. Calhoun, F. A. Honore. IEEE JSC, 2004
9. Sleep Transistor Sizing Using Timing Criticality and Temporal Currents", Proc. Asia South Pacific Design Automation Conference (ASPDAC), to appear, Jan. 2005.